AMENDMENTS TO THE SPECIFICATION

Please replace the below indicated paragraphs with the replacement paragraphs identified with respect to U.S. Patent Application Publication US 2005/0174188 A1 (this application):

Please replace paragraph [0034] with the following replacement paragraph:

[0034] Moreover, a decompressing device of the present invention is comprising delay circuits of several stages into which discrete thinned-out data produced by a compressing device ~~claimed in claim 1~~ can be inputted, each of the delay circuits delaying the inputted thinned-out data in sequence, and a multiplying/adding circuit for performing weighted addition on data outputted from each of the delay circuits, the weighted addition being performed according to a value of a digital basic function, whereby interpolation data for the thinned-out data is produced.

Please replace paragraph [0038] with the following replacement paragraph:

[0038] Another aspect of the present invention is comprising first interpolating means for performing an interpolation process with respect to thinned-out data produced by a compressing device ~~claimed in claim 9~~, in which in the interpolation process, timing data and amplitude data on each sampling point are used to produce first interpolation data for interpolating between one amplitude data and the other amplitude data which have a time interval indicated by the timing data, and second interpolating means for producing second interpolation data for the produced first interpolation data by performing a further interpolation process with respect to the produced first interpolation data, in which in the further interpolation process, weighted addition is performed on interpolation data on a target sample point and interpolation data on several sample points around the target sample point, the weighted addition being performed according to a value of a digital basic function.

Please replace paragraph [0040] with the following replacement paragraph:

[0040] Another aspect of the present invention is further comprising interpolating means for performing an interpolation process with respect to discrete thinned-out data produced by a compressing device ~~claimed in claim 15~~ to produce interpolation data for the discrete thinned-out data, wherein in the interpolation process, weighted addition is performed on thinned-out data on a target sample point and thinned-out data on several sample points around the target sample point, the weighted addition being performed according to a value of a digital basic function.

Please replace paragraph [0047] with the following replacement paragraph:

[0047] Another aspect of the present invention is further comprising the steps of performing a zero decompressing process with respect to thinned-out data produced by a compressing method ~~claimed in claim 36~~, in which when a -0 value is detected in the thinned-out data, a corresponding number of successive zero data are reproduced through the zero decompressing process.

Please replace paragraph [0048] with the following replacement paragraph:

[0048] Further, a program of the present invention is, for example, a compressing program for causing a computer to function as ~~each~~ various means ~~as set forth in claim 9~~, a compressing program for causing the computer to perform the operating steps of a compressing method ~~as set forth in claim 24~~, a decompressing program for causing the computer to function as ~~each~~ various means ~~as set forth in claim 66~~, or a decompressing program for causing the computer to perform the operating steps of ~~the~~ a decompressing method ~~as set forth in claim 77~~.

Please replace paragraph [0049] with the following replacement paragraph:

[0049] Further, a record medium readable by a computer according to the present invention is characterized by recording, for example, a program for causing a computer to function as ~~each~~ various means ~~as set forth in claim 9~~, a program for causing the computer to perform the operating steps of ~~the~~ a compressing method ~~as set forth in claim 24~~, a program for causing the computer to function as ~~each~~ various means ~~as set forth in claim 66~~, or a program for

causing the computer to perform the operating steps of a decompressing method ~~as set forth in claim 77~~.

Please replace paragraph [0107] with the following replacement paragraph:

[0107] A thinning-out circuit of the first stage operates on a clock 8 CK of a reference frequency (e.g., 44.1 KHz). D-type flip-flops 1_{-1}, 2_{-1}, 3_{-1}, and 4_{-1} of four stages delay sampling data (e.g., 16 bits), which are inputted in sequence in a discrete manner, by one clock 8 CK of the reference frequency one by one. These D-type flip-flops 1_{-1} to 4_{-1} correspond to delay circuits of four stages ~~in claim 2~~.

Please replace paragraph [0108] with the following replacement paragraph:

[0108] An adder 5_{-1} adds data retrieved from the output taps of the D-type flip-flops 2_{-1} and 3_{-1} of the second and third stages. An adder 6_{-1} multiplies the output data from the adder 5_{-1} by 9. The adder 5_{-1} and the adder 6_{-1} correspond to a first multiplying/adding circuit ~~described in claim 3~~.

Please replace paragraph [0109] with the following replacement paragraph:

[0109] An adder 7_{-1} adds data retrieved from the output taps of the D-type flip-flops 1_{-1} and 4_{-1} of the first and fourth stages. A multiplier 8_{-1} multiplies the output data from the adder 7_{-1} by $_{-1}$. The adder 7_{-1} and the multiplier 8_{-1} correspond to a second multiplying/adding circuit ~~described in claim 3~~.

Please replace paragraph [0110] with the following replacement paragraph:

[0110] An adder 9_{-1} adds the output data from the two multipliers 6_{-1} and 8_{-1}. A multiplier 10_{-1} multiplies the output data from the adder 9_{-1} by {fraction (1/16)}. The adder 9_{-1} and the multiplier 10_{-1} correspond to a third multiplying/adding circuit ~~described in claim 3~~.

Please replace paragraph [0116] with the following replacement paragraph:

[0116] An oversampling circuit of the first stage operates on a clock CK whose frequency (5.5125 KHz) is one eighth of the reference frequency. D-type flip-flops 21_{-1}, 22_{-1}, and 23_{-1} of three stages delay thinned-out data one by one, which are inputted in sequence in a discrete manner, by one clock CK. These D-type flip-flops 21_{-1}, 22_{-1}, and 23_{-1} correspond to delay circuits of three stages ~~in claim 52~~.

Please replace paragraph [0118] with the following replacement paragraph:

[0118] The output data from the D-type flip-flops 21_{-1} of the first stage is inputted to one of the input terminals of an AND gate 25_{-1} via a multiplier 24_{-1} of $_{-1}$ time ~~(corresponding to a first multiplier of claim 53)~~ and is inputted to one of the input terminals of an AND gate 26_{-1} without passing through a multiplier (corresponding to +1 time). An inversion clock CK passing through an inverter 27_{-1} is inputted to the other input terminal of the AND gate 25_{-1} is fed with. Further, the clock CK is inputted to the other input terminal of the AND gate 26_{-1}.

Please replace paragraph [0119] with the following replacement paragraph:

[0119] The output data from the two AND gates 25_{-1} and 26_{-1} are outputted via an OR gate 28_{-1}. Thus, thinned-out data of +1 time is outputted from the OR gate 28_{-1} when the clock CK is "H". Further, thinned-out data of -1 time is outputted from the OR gate 28_{-1} when the clock CK is "L". Namely, the first term of equation (12) is obtained when the clock CK is "H", and the first term of equation (13) is obtained when the clock CK is "L". A first switching circuit ~~of claim 53~~ is constituted by the two AND gates 25_{-1} and 26_{-1}, the inverter 27_{-1}, and the OR gate 28_{-1}.

Please replace paragraph [0120] with the following replacement paragraph:

[0120] The output data from the D-type flip-flop 22_{-1} of the second stage is outputted via a multiplier 29_{-1} of +8 times (corresponding to a second multiplier ~~of claim 53~~). As shown in equations (12) and (13), since the ".+-." sign of the second term is not changed in both of the

equations, unlike the first term, a circuit for switching the sign based on the clock CK is not necessary.

Please replace paragraph [0121] with the following replacement paragraph:

[0121] The output data from the D-type flip-flops 23_{-1} of the third stage is inputted to one of the input terminals of an AND gate 31_{-1} via a multiplier 30_{-1} of -1 time (corresponding to a third multiplier ~~of claim 53~~) and is inputted to one of the input terminals of an AND gate 32_{-1} without passing through a multiplier (corresponding to +1 time). The clock CK is inputted to the other input terminal of the AND gate 31_{-1}. Further, the inversion clock CK passing through an inverter 33_{-1} is inputted to the other input terminal of the AND gate 32_{-1}.

Please replace paragraph [0122] with the following replacement paragraph:

[0122] The output data from the two AND gates 31_{-1} and 32_{-1} are outputted via an OR gate 34_{-1}. Thus, thinned-out data of -1 time is outputted from the OR gate 34_{-1} when the clock CK is "H". Further, thinned-out data of +1 time is outputted from the OR gate 34_{-1} when the clock CK is "L". Namely, the third term of equation (12) is obtained when the clock CK is "H", and the third term of equation (13) is obtained when the clock CK is "L". A second switching circuit ~~of claim 53~~ is constituted by the two AND gates 31_{-1} and 32_{-1}, the inverter 33_{-1}, and the OR gate 34_{-1}.

Please replace paragraph [0123] with the following replacement paragraph:

[0123] The output data from the OR gate 28_{-1}, the output data from the eight-times multiplier 29_{-1}, and the output data from the OR gate 34_{-1} are all added by two adders 35_{-1} and 36_{-1} (corresponding to an adder ~~of claim 53~~). Thus, the arithmetic result of equation (12) is outputted from the adder 36_{-1} when the clock CK is "H", and the arithmetic result of equation (13) is outputted from the adder 36_{-1} when the clock CK is "L".

Please replace paragraph [0160] with the following replacement paragraph:

[0160] A decompressing device of FIG. 10 comprises D-type flip-flops 81, 82, 83, and 84 of four stages for delaying thinned-out data, which are inputted in sequence, by one clock CK one by one. The D-type flip-flops 81 to 84 of four stages correspond to delay circuits of four stages ~~in claim 59~~.

Please replace paragraph [0193] with the following replacement paragraph:

[0193] The thinning-out circuit in the first stage operates on a clock 8 CK of a reference frequency (e.g., 44.1 KHz). D-type flip-flops 101_{-1}, 102_{-1}, 103_{-1}, 104_{-1}, 105_{-1}, 106_{-1}, and 107_{-1} of seven stages delay sampling data (e.g., 16 bits), which are inputted in sequence in a discrete manner, by one clock 8 CK of the reference frequency one by one. These D-type flip-flops 101_{-1} to 107_{-1} correspond to delay circuits of seven stages ~~in claim 5~~.

Please replace paragraph [0194] with the following replacement paragraph:

[0194] An adder 108_{-1} adds data retrieved from the output taps of the D-type flip-flops 101_{-1} and 107_{-1} in the first and seventh stages. A multiplier 109_{-1} multiplies the output data from the adder 108_{-1} by -1. The adder 108_{-1} and the multiplier 109_{-1} correspond to a first multiplying/adding circuit ~~in claim 6~~.

Please replace paragraph [0195] with the following replacement paragraph:

[0195] An adder 110_{-1} adds data retrieved from the output taps of the D-type flip-flops 103_{-1} and 105_{-1} in the third and fifth stages. A multiplier 111_{-1} multiplies the output data from the adder 110_{-1} by 9. The adder 110_{-1} and the multiplier 111_{-1} correspond to a second multiplying/adding circuit ~~in claim 6~~.

Please replace paragraph [0197] with the following replacement paragraph:

[0197] Adders 113_{-1} and 114_{-1} add output data from the above three multipliers 109_{-1}, 111_{-1}, and 112_{-1}. A multiplier 115_{-1} multiplies the output data from the adder 114_{-1} by 1/32. The

adders 113_{-1}, 114_{-1}, and the multiplier 115_{-1} correspond to a third multiplying/adding circuit ~~described in claim 6~~.

Please replace paragraph [0202] with the following replacement paragraph:

[0202] An oversampling circuit of the first stage operates on a clock CK whose frequency (5.5125 KHz) is one eighth of the reference frequency. D-type flip-flops 121_{-1}, 122_{-1}, 123_{-1}, 124_{-1}, and 125_{-1} of five stages delay thinned-out data (e.g., 16 bits), which is inputted in sequence, by one clock CK one by one. These D-type flip-flops 121_{-1} to 125_{-1} correspond to delay circuits of five stages ~~in claim 63~~.